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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/045,913	01/09/2002	Rana P. Singh	SC11448TP P01	3167

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EXAMINER
GEBREMARIAM, SAMUEL A

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 04/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/045,913	SINGH ET AL.
	Examiner	Art Unit
	Samuel A Gebremariam	2811

-- The MAILING DATE of this communication appears on the cover sheet with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 February 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,15-34 and 38-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,15-34,38-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1, 2, 5, 8-10,15, 19 and 23-25,are rejected under 35 U.S.C. 102(e) as being anticipated by Shiozawa et al., US patent No. 6,245,641.

Regarding claims 1 and 15, Shiozawa teaches (figs. 2-9) a method for forming a semiconductor device structure in a semiconductor layer, comprising: forming a first trench (4b) of a first width and a second trench (4a) of a second width in the semiconductor layer; growing a first insulator liner (5b) in the first trench and a second insulator liner (5a and 8) in the second trench; forming a mask (11) over the second trench (4a); etching at least a portion of the first insulator liner while the mask is over the second trench; removing the mask; and depositing an insulating layer (6) in the first trench and the second trench.

Shiozawa teaches more than one layer of oxide liner. Regarding claim 2, Shiozawa teaches (fig. 3) the entire claimed process of claim 1 above including the first width (4b) is less than the second width (4a).

Regarding claim 5, Shiozawa teaches (figs. 4 and 5) the entire claimed process of claim 1 above including step of forming first insulator liner and the second insulator liner comprises growing oxide in the first trench and the second trench.

Regarding claim 8, Shiozawa teaches (fig. 8, col. 10, line 36-44) the entire claimed process of claim 1 above including the insulator layer comprises high-density plasma oxide fill.

Regarding claim 9, Shiozawa teaches (fig. 3) the entire claimed process of claim 1 above including forming a barrier layer (3a-3d) and a stress relief layer (2a-2d) over the semiconductor layer in areas adjacent to the first trench and the second trench.

Regarding claim 10, Shiozawa teaches (figs. 2 and 3) the entire claimed process of claim 1 above including a pad nitride and pad oxide over the semiconductor layer prior to forming the first trench and the second trench, and wherein the step of forming the first trench and the second trench comprises etching through selected portions of the pad nitride and the pad oxide and into the semiconductor layer (col. 9, line 54 to 63).

Regarding claims 19, 24 and 25, Shiozawa teaches (figs. 2, 3 and 7) the entire claimed process of claims 1, 5 and 9 above including the step of forming the first insulator liner (5b, 8) and the second insulator liner (5a and 8) comprises growing oxide in the first trench (4b) and the second trench (4a).

Regarding claims 26 and 27, Shiozawa teaches (figs. 3 and 7) the entire claimed process of claim 1 above including the step of forming a mask (11) over the second trench (4a) prior to the step of etching and removing the mask prior to the step of depositing.

Regarding claim 29, Shiozawa teaches (figs. 12 and 13) forming a first trench (4b) of a first width and a second trench (4a) of a second width in the semiconductor layer; growing a first insulator liner (5b and 8) in the first trench and a second insulator liner (5a and 8) in the second trench; etching a portion of the first insulator liner and a portion of the second insulator liner and depositing an insulating layer (6) in the first trench and the second trench.

The claim does not preclude removing the entire portion of the first liner.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3, 4, 6, 16, 17, 18, 22, 28, 32, 40 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiozawa et al.

Regarding claim 3, Shiozawa teaches (fig. 7) the entire claimed process of claim 1 above except explicitly stating the step of etching comprises completely removing the first insulator liner.

It is conventional in the art to completely remove oxide liners in a trench after forming them.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to completely remove the first liner oxide taught by Shiozawa since

it oxide liners are some times formed to minimize the damage done during etching process and removed afterwards.

Regarding claims 4 and 22, Shiozawa teaches substantially the entire claimed process of claims 1 and 15 above except explicitly stating that the step of etching results in leaving at least portion of the first and second insulator liner as claimed.

Parameters such as thickness in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device characteristics.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to vary the thickness of the oxide liner as claimed in order to form good isolation.

Regarding claim 32, Shiozawa teaches substantially the entire claimed process of claim 29 above including the first insulator liner (5b and 8) and the second insulator liner (5a and 8) comprises thermal oxide (col. 10, line 1-4).

Regarding claim 33, Shiozawa teaches substantially the entire claimed process of claim 29 above including the step of depositing comprises filling the first trench and second trench (fig. 15).

Regarding claim 34, Shiozawa teaches (fig. 8, col. 10, line 36-44) substantially the entire claimed process of claim 29 above including the insulating layer (6) comprises high-density plasma oxide (fig. 15).

Regarding claims 6, 16, 17, 30, 31 Shiozawa teaches substantially the entire claimed process of claims 1,15 and 29 above except explicitly stating that the step of

etching comprises a wet etch where the process comprises dipping the semiconductor device structure in hydrofluoric acid.

It is conventional and also taught by Shiozawa using wet etch process for removing portion of the oxide layer (8) in figure 12. Also hydrofluoric acid is a widely known etchant of oxide layer.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the conventional etchant HF in the conventional process of using wet etch for removing oxide layer taught by Shiozawa in order to remove portion of the oxide liner (fig. 12).

Claims 7, 18, 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiozawa in view of Lee US patent No. 5,994,201.

Regarding claims 7 and 18, Shiozawa teaches substantially the entire claimed process of claims 1 and 15 above except explicitly stating that the step of etching comprises applying etch chemistry to the semiconductor device.

The use of dry etching for removing oxide layer is a conventional process that is widely known and also taught by Lee (col., 6, lines 6-8) for removing oxide layer (206).

It would have been obvious to one of ordinary skill in the art at the time the invention was made in corporate the conventional process of using dry etching process taught by Lee in the process of Shiozawa in order to etch the oxide liner as claimed.

Regarding claim 20, Shiozawa teaches substantially the entire claimed process of claims 1 and 15 above including the semiconductor layer has a top surface.

Shiozawa does not teach the step of forming the first insulator liner and the second insulator liner comprises rounding of the corner of the second.

It is conventional in the art to form trench corners that are rounded.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to forming rounded corners of trenches in the process steps of Shiozawa since round corners prevent hump currents generated by electric field concentrated at sharp corners that in turn prevent leakage current.

Regarding claim 21, Shiozawa teaches substantially the entire claimed process of claim 20 above including the corner is a semiconductor.

The modified structure of Shiozawa would inherently have a rounded corner that is semiconductor.

Claims 38-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiozawa in view of Koike US patent No. 5,578,518.

Regarding claims 38-41, Shiozawa teaches substantially the entire claimed process of claims 20, 29, 32, 33 and 34 above except explicitly stating growing a first insulator liner in the first trench and a second insulator liner in the second trench to achieve a radius of curvature of at least 200 Angstroms in the first and second corner.

Koike teaches (see abstract) rounding of isolation trenches to achieve a radius of curvature of not less than 500 angstroms.

Furthermore parameters such as radius of curvature in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device characteristics.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the radius of curvature of corners of the first and second trenches in the process of Shiozawa as taught by Koike since rounding of the edges prevents the concentration of electric field in the edge portion of the trench isolation resulting in the prevention of the lowering of the threshold voltage (col. 2, lines 43-47, Koike).

Response to Arguments

3. Applicant's arguments filed 2/5/03 have been fully considered but they are not persuasive. Applicant argues that the oxide layer of Shiozawa is deposited by CVD and not grown. The process of depositing an oxide layer on top of a substrate is the same as growing an oxide layer using CVD deposition. Applicant does not explicitly state that the oxide layer in the claims is thermally grown oxide layer.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel Admassu Gebremariam whose telephone number is 703 305 1913. The examiner can normally be reached on 8:00am-4: 30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 305-7646. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Samuel Admassu Gebremariam
April 21, 2003

Steven Loke